IN THE CLAIMS

1. A method of fabricating a high dielectric constant (high-k) capacitor structure, said method comprising:

depositing an adhesion layer on a SiO_2 substrate, said adhesion layer being selected from the group consisting of Si, Al, Al plus TiN, and SiO_2; and

depositing a noble metal bottom electrode on said adhesion layer.

2. The method of claim 1 further comprising:

depositing a high-k dielectric material on said bottom electrode;

depositing a top electrode on said high-k dielectric layer;

patterning said top electrode and said high-k dielectric layer;

depositing an insulation layer thereon;

opening vias to said top electrode in the insulation layer;

depositing a metal pad layer in said vias and atop said insulation layer; and

patterning the metal pad layer.

3. The method recited in claim 1 wherein said bottom electrode is Pt

4. The method recited in claim 2 wherein said top electrode is Pt.

5. The method recited in claim 2 wherein said insulation layer is SiO_2.

6. The method recited in claim 2 wherein said metal pad layer is Al or W.

7. A method of fabricating a three-dimensional capacitor structure, comprising the steps of:

depositing a SiO_2 layer on a substrate;

opening vias in said SiO_2 layer;

depositing polycrystalline Si into said vias;

planarizing and recessing back said polycrystalline Si to form poly plugs in said vias;

depositing a barrier layer in said vias atop said poly plugs;

planarizing said barrier layer;

depositing an adhesion layer atop said barrier layer and said SiO_2 layers, said adhesive layer being selected from the group consisting of Si, Al, Al plus TiN, and IrO_2; and

depositing a noble metal bottom electrode on said adhesive layer.

8. The method recited in claim 7 wherein said adhesion layer is conductive.

9. The method recited in claim 8 wherein said adhesion layer is IrO_2.

10. The method recited in claim 7 wherein said adhesion layer is a non-conductive layer, and said method further comprises:

removing a portion of said adhesion layer that is above said barrier layer before depositing said bottom electrode.

11. The method recited in claim 7 wherein said bottom electrode is Pt.

12. The method recited in claim 7 further comprising:

patterning said bottom electrode to form a three-dimensional structure;

depositing a high-k dielectric layer thereon; and

depositing a top electrode on said high-k dielectric layer.

13. The method recited in claim 12 further comprising:

depositing and patterning a SiO_2 layer to form a three-dimensional structure prior to depositing said adhesion layer.

14. The method recited in claim 13 further comprising:

removing a top planar part of said bottom electrode;

depositing a high-k dielectric layer; and

depositing a top electrode

15. The method recited in claim 14 wherein said bottom and top electrodes are Pt.